In the Claims

Please replace all prior versions, and listings, of claims in the application with the following list of claims:

1. (Previously presented) A controller for a plurality of power supplies, the controller comprising:

a logic core having a plurality of inputs and a plurality of outputs for supplying signals to control said power supplies; and

a memory;

wherein the controller functions as a state machine and upon the transition from a state to a succeeding state the operation of the logic core is modified in accordance with data held in the memory, such that the inputs selected for monitoring by the logic core can be varied as the controller changes state.

2. (Previously presented) A controller as claimed in claim 1, in which the logic core represents a state having up to three outputs.

3. (Previously presented) A controller as claimed in claim 1, in which the logic core includes a fault detector.

4. (Previously presented) A controller as claimed in claim 3, in which the fault detector has a plurality of inputs and a lesser number of outputs.

5. (Previously presented) A controller as claimed in claim 4, in which the fault detector has a single output.

6. (Previously presented) A controller as claimed in claim 4, in which at least one input of the fault detector is associated with a respective input detector which is responsive to at least one of:

a. a mask/select control signal for determining whether an input signal at a signal input of the input detector should be taken into consideration by the fault detector; and

b. an invert signal for causing an output signal from the input detector to be inverted with respect to the input signal.

7. (Previously presented) A controller as claimed in claim 4, in which at least one input detector has multiple signal inputs and it is responsive to the order in which the signal inputs change.

8. (Previously presented) A controller as claimed in claim 3, in which the fault detector includes combinational logic for combining its inputs in a logical OR.

9. (Previously presented) A controller as claimed in claim 5 in which an output of the fault detector is supplied to a device arranged in a first mode to pass the output of the fault detector in a non-inverted state and in a second mode to invert the output of the fault detector.

10. (Previously presented) A controller as claimed in claim 1 in which the logic core includes a combinational logic unit having a plurality on inputs and a single output, and wherein at least one of the inputs is selectively maskable and invertable such that the combinational logic unit can be arranged to look for the occurrence of a plurality of input signals being in a predetermined state, and to assert a first predetermined output signal when the input signals are in the predetermined state and a second predetermined output signal when the input signals are not in the predetermined state.

11. (Previously presented) A controller as claimed in claim 1 in which the logic core comprises a sequence detector.

12. (Previously presented) A controller as claimed in claim 11, wherein the sequence detector has a plurality of inputs and a lesser number of outputs.

13. (Previously presented) A controller as claimed in claim 12, in which the sequence detector has a single output.

14. (Previously presented) A controller as claimed in claim 12, in which the sequence detector comprises a multiplexer responsive to a selection control word to select only one of the plurality of inputs.

15. (Previously presented) A controller as claimed in claim 11 in which the sequence detector includes a device arranged in a first mode to pass a signal to or from the multiplexer in a non-inverted state and in a second mode to invert the signal.

16. (Previously presented) A controller as claimed in claim 11 in which the sequence detector further includes a sequence timer arranged to assert an output signal only when an input condition monitored by the sequence detector has been in a predetermined state for a predetermined period.

17. (Previously presented) A controller as claimed in claim 16, in which the sequence timer is programmable.

18. (Previously presented) A controller as claimed in claim 1, in which the logic core comprises a time out circuit having a time out timer selectively arranged to assert an output a predetermined period after the logic core has entered a state.

19. (Previously presented) A controller as claimed in claim 18, in which the time out timer is programmable.

20. (Previously presented) A controller as claimed in claim 1, in which the memory is programmable.

21. (Previously presented) A controller as claimed in claim 20, in which the memory is user programmable.

22. (Previously presented) A controller as claimed in claim 20 in which the memory is non-volatile.

23. (Previously presented) A controller as claimed in claim 1, in which the memory holds data which is a state control word comprising a least one of the following items:

a. output data defining the condition of at least one output upon entry into a state;

b. data for controlling a fault detector, and in particular data defining whether an input of the fault detector is to be masked and data identifying the next state to be executed if a fault condition is determined by the fault detector, and

c. data for controlling a sequence detector, and in particular data defining which input of the sequence detector is to be monitored and data identifying the next state to be executed if the sequence detector determines that a condition it is monitoring is satisfied.

24. (Previously presented) A controller as claimed in claim 23, in which the memory further includes data for setting a duration timed by a time out timer and data identifying the next state to be executed after the time out timer has timed out and triggered a state change.

25. (Cancelled)

26. (Previously presented) An integrated circuit including a controller as claimed in claim 1.

27-38. (Cancelled)

39. (New) A method for controlling a plurality of power supplies, comprising:

providing a logic core having a plurality of inputs and a plurality of outputs which supply signals for controlling said power supplies;

providing a memory; and

operating the logic core as a state machine and upon transition from a state to a succeeding state, modifying the operation of the logic core in accordance with data held in the memory, such that the inputs selected for monitoring by the logic core can be varied as the controller changes state.

40. (New) The method of claim 39, wherein the logic core is operated to represent a state having up to three outputs.

41. (New) The method of claim 39, further including operating the logic core to perform a fault detection function.

42. (New) The method of claim 41, wherein the logic core, when operated as a fault detector, has a plurality of inputs and a lesser number of outputs.

43. (New) The method of claim 42, in which the fault detector has a single output.

44. (New) The method of claim 43 further including supplying a fault detector output to a device arranged in a first mode to pass the output of the fault detector in a non-inverted state and in a second mode to invert the output of the fault detector.

45. (New) The method of claim 42, further comprising providing an input detector, associated with the logic core when it is operated as a fault detector, and which is responsive to at least one of:

a. a mask/select control signal for determining whether an input signal at a signal input of the input detector should be taken into consideration by the fault detector; and

b. an invert signal for causing an output signal from the input detector to be inverted with respect to the input signal.

46. (New) The method of claim 42 in which at least one input detector has multiple signal inputs and is responsive to the order in which the signal inputs change.

47. (New) The method of claim 41 wherein providing a fault detector includes providing combinational logic for combining its inputs in a logical OR function.

48. (New) The method of claim 39, wherein providing the logic core includes providing a combinational logic unit therein having a plurality of inputs and a single output, at least one of the inputs being selectively maskable and invertable such that the combinational logic unit is configurable to look for the occurrence of a plurality of inputs in a predetermined state and to assert a first predetermined output signal when the input signals are in the predetermined state and the second predetermined output signal when the input signals are not in the predetermined state.

49. (New) The method of claim 39 wherein providing the logic core includes providing a sequence detector.

50. (New) The method of claim 49 wherein providing a sequence detector includes providing a sequence detector having a plurality of inputs and a lesser number of outputs.

51. (New) The method of claim 50 wherein the sequence detector has a single output.

52. (New) The method of claim 50 wherein the sequence detector comprises a multiplexor responsive to a selection control word to select only one of the plurality of inputs.

53. (New) The method of claim 49 in which the sequence detector includes a device arranged in a first mode to pass the signal to or from the multiplexor in a non-inverted state and in a second mode to invert the signal.

54. (New) The method of claim 49 in which the sequence detector further includes a sequence timer arranged to assert an output signal only when an input condition monitored by the sequence detector has been in a predetermined state for a predetermined period.

55. (New) The method of claim 54 in which the sequence timer is programmable.

56. (New) The method of claim 39 wherein providing a logic core includes providing a logic core comprising a time out circuit having a time out timer selectively arranged to assert an output a predetermined period after the logic core has entered a state.

57. (New) The method of claim 56 in which the time out time is programmable.

58. (New) The method of claim 39 in which the memory is programmable.

59. (New) The method of claim 58 in which the memory is user programmable.

60. (New) The method of claim 58 in which the memory is non-volatile.

61. (New) The method of claim 39 wherein the memory is adapted to hold data which is a state control word comprising at least one of the following items:

a. output data defining the condition of at least one output upon entry into a state;

b. data for controlling a fault detector, and in particular data defining whether an input of the fault detector is to be masked and data identifying the next state to be executed if a fault condition is determined by the fault detector, and

c. data for controlling a sequence detector, and in particular data defining which input of the sequence detector is to be monitored and data identifying the next state to be executed if the sequence detector determines that a condition it is monitoring is satisfied.

62. (New) The method of claim 61 wherein the memory further is adapted to include data for setting a duration timed by a time out timer and data identifying the next state to be executed after the time out timer has timed out and triggered a state change.